VITA 62 Power Supply

VIT028x6U1000y000

VITA 62 DC-DC Converter

Features & Benefits

- Open VPX – VITA 62
- 18 – 42V input voltage range
- 1000W output power
- 6U Open VPX power supply
- Conduction cooled
- I^2C monitoring and control
- Input voltage reverse-polarity protection
- Remote voltage sense: VS1, VS3
- Parallel operation capable with proprietary wireless current sharing
- Overcurrent, overvoltage and overtemperature protections
- IPC 610 class 3
- No aluminum electrolytic capacitors
- Enable, inhibit, system reset and power fail controls
- Accredited laboratory military standard compliance: [a]
  - MIL-STD-704F
  - MIL-STD-461G
  - MIL-STD-810G
  - MIL-STD-1275E
  - RTCA/DO-160G

Typical Applications

- VPX power modules
- Avionics
- Shipborne electronics

Product Description

The Vicor VITA 62 power supply is a COTs power supply that is designed for 6U Open VPX systems. The module utilizes Vicor proprietary technology to enable high efficiency and power density for this highly rugged, conduction-cooled model.

Up to four power supplies can be paralleled to increase output power capability of VS1, VS3 outputs with proprietary wireless current sharing.

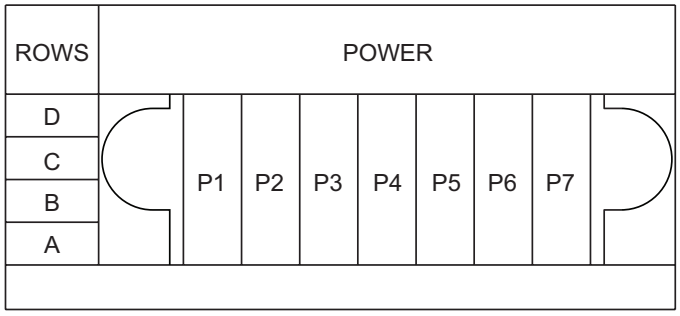
Conventional current-share pins are eliminated.

Current share accuracy is ±2A.

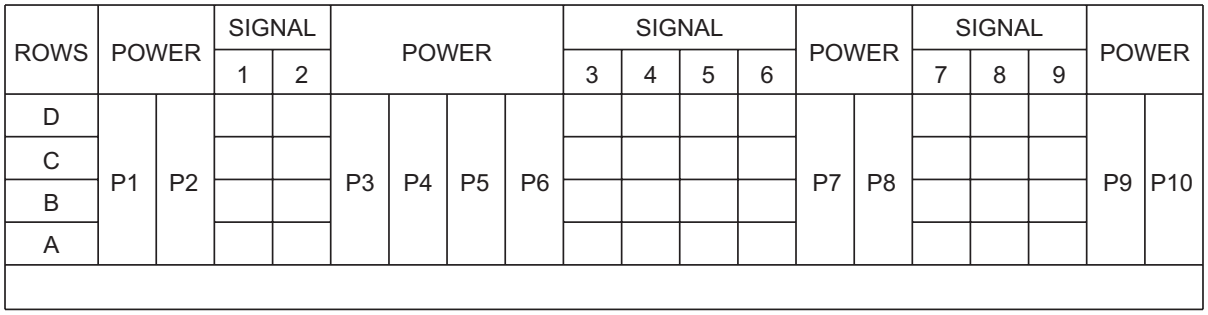
[a] See detailed specifications; contact Vicor Applications Engineering for report details.

Note: Product images may not highlight current product markings.

Connector Pin Configurations



6U P0 Connector



6U P1 Connector

Note: See mechanical drawing on page 30 for connector information.

Connector Pin Descriptions

Pin	Function / Name	Description
P0 Connector		
P1	CHASSIS	Chassis
P2	No Connection	No connection
P3	No Connection	No connection
P4	–DC_IN	V_{IN-}
P5	–DC_IN	V_{IN-}
P6	+DC_IN	V_{IN+}
P7	+DC_IN	V_{IN+}

Connector Pin Descriptions (Cont.)

Pin	Function / Name	Description
P1 Connector		
P1	POWER_RETURN	Common output return pin, each pin is rated for 40A
P2	VAUX2	+3.3V main output voltage (rated for 0 – 30A_{DC})
A1	UD3	No connection
B1	UD4	No connection
C1	UD5	No connection
D1	UD6	No connection
A2	NC	No Connection
B2	FAIL*	When any of the outputs is not within specifications, FAIL* signal will be driven low to indicate a failure
C2	INHIBIT*	Input control signal as defined in VITA 62, reference to SIGNAL_RETURN
D2	ENABLE*	Input control signal as defined in VITA 62, reference to SIGNAL_RETURN
P3	POWER_RETURN	Common output return pin, each pin is rated for 40A
P4	POWER_RETURN	Common output return pin, each pin is rated for 40A
P5	VS3	+5V main output voltage (rated for 0 – 32A_{DC})
P6	VS3	
A3	UD2	No connection
B3	VAUX3	+12V AUX output voltage (rated for 0 – 1A_{DC})
C3	NC	No connection
D3	NC	No connection
A4	GA3*	Geographical address defined by VITA 46.11
B4	GA2*	Geographical address defined by VITA 46.11
C4	GA1*	Geographical address defined by VITA 46.11
D4	GA0*	Geographical address defined by VITA 46.11
A5	GAP*	Geographical address defined by VITA 46.11
B5	GA4*	Geographical address defined by VITA 46.11
C5	SM0	Primary I^2C™ communication bus (clock line)
D5	SM1	Primary I^2C communication bus (data line)
A6	SM2	Redundant I^2C communication Bus (clock line)
B6	SM3	Redundant I^2C communication Bus (data line)
C6	VAUX1	–12V AUX output voltage (rated for 0 – 1A_{DC})
D6	SYSRESET*	System reset is actively low. It will float when all outputs are within specifications
P7	POWER_RETURN	Common output return pin, each pin is rated for 40A
P8	POWER_RETURN	Common output return pin, each pin is rated for 40A
A7	VS1_SHARE	No connection
B7	VS2_SHARE	No connection
C7	VS3_SHARE	No connection
D7	SIGNAL_RETURN	Ground pin for control signals
A8	VS1_SENSE-RTN	Must be connected to POWER_RETURN at connector or remotely
B8	VS2_SENSE-RTN	
C8	VS3_SENSE-RTN	Must be connected to POWER_RETURN at connector or remotely
D8	UD1	No connection
A9	VS1_SENSE+	Must be connected to +12V main output at connector or remotely
B9	VS2_SENSE+	
C9	VS3_SENSE+	Must be connected to +5V main output at connector or remotely
D9	UD0	No connection
P9	VS2	+12V main output voltage (rated for 0 – 70A_{DC})
P10	VS1	

Part Ordering Information

Part Number	Product Grade	Conformal Coating	Factory-Configured Options
VIT028**H**6U1000**C000**	**H** = –40 to 85°C	**C** = Coated	**000** = Programmable [b]

[b] Factory option 000 units can be set by the user to parallel ready or standalone operation only via I²C™.
See I²C user guide for information on changing the unit from Parallel operation to Standalone. By default, units are set to parallel from the factory.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
Total Output Power	Combined outputs for all rails		1000	W
Operational Input Voltage	+IN to –IN, 100V 50ms operation MIL-STD-1275E surge only	–0.5	100	V
Operating Temperature	Measured at card edge	–40	85	°C
Storage Temperature		–40	125	
Isolation Voltage IN to OUT			500	V_{DC}
Isolation Voltage IN to CASE			500	V_{DC}
Isolation Voltage OUT to CASE			100	V

Electrical Characteristics

All data at nominal line and nominal load unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Overall System Characteristics						
System Efficiency		Nominal line, 25% aggregate loads		85.1		%
		Nominal line, 50% aggregate loads		88.1		
		Nominal line, 100% aggregate loads		89		
Power Input Characteristics						
Operating Input Voltage Range	V_{IN}		18	28	42	V
Input Current (No Load)	I_{IN-NL}	28V Input, enable asserted, inhibit de-asserted		0.4	0.8	A
Inrush Current	I_{INRUSH}	Peak no load, nominal line, high line; see Figure 5		60	120	A
Power On to +3.3V_{AUX} Output Delay		If ENABLE* is tied to signal ground	300	400	500	ms
Power Output Characteristics						
Output Power Limit (During Starting Disturbance)		Initial engagement surge, 12 – 16V, 1s per MIL-STD-1275E, see Figure 28			500	W
		Cranking surge, 16 – 18V, 30s per MIL-STD-1275E, see Figure 28			1000	
Main Outputs						
VS1: +12V Output						
Output Voltage Set Point	$V_{SET-VS1}$	VS1 output is set to $V_{SET-VS1}$ at no load and adjusts the output voltage as a function load, where: $V_{OUT\_VS1} = V_{SET-VS1} – (0.240V \bullet (I_{OUT} / I_{R-VS1}))$	12.09	12.12	12.15	V
Output Regulation Over Line & Load				240	270	mV
Output Voltage Ripple / Noise		Nominal line from 3.5A load to full load		50	120	mV_{P-P}
Rated Output Current	I_{R-VS1}				70	A
Maximum Operating Transmission Voltage Drop	V_{TD-VS1}				0.5	V
Maximum Output Capacitance	C_{O-VS1}				9	mF
Soft-Start Ramp Time	t_{SS-VS1}	All full load with max C_{O-VS1}	5			ms

Electrical Characteristics (Cont.)

All data at nominal line and nominal load unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Main Outputs (Cont.)						
VS3: +5V Output						
Output Voltage Set Point	$V_{SET-VS3}$	VS3 output is set to $V_{SET-VS3}$ at no load and adjusts the output voltage as a function load, where: $V_{OUT\_VS3} = V_{SET-VS3} – (0.100V \bullet (I_{OUT} / I_{R-VS3}))$	5.01	5.05	5.07	V
Output Regulation Over Line & Load				100	130	mV
Output Voltage Ripple / Noise		Nominal line over load range, 20MHz BW; measured with 1µF and 10µF ceramic capacitor		25	50	mV_{P-P}
Rated Output Current	I_{R-VS3}				32	A
Maximum Operating Transmission Voltage Drop	V_{TD-VS3}				0.5	V
Maximum Output Capacitance	C_{O-VS3}				9	mF
Soft-Start Ramp Time	t_{SS-VS3}	All full load with max C_{O-VS3}	5			ms
VS2: +3.3V Output						
• The Power Supply does not provide a 3.3V main output; the VS2 contacts are used to increase current carrying capability of the +12V main output (VS1). • The +3.3V VAUX2 output is a higher current output with a 30A capability.						

Electrical Characteristics (Cont.)

All data at nominal line and nominal load unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Auxiliary Outputs						
VAUX1: –12V Output						
Output Voltage Set Point	$V_{SET-VAUX1}$		11.8	12.2	12.3	V
Output Regulation Over Line & Load					200	mV
Output Voltage Ripple / Noise		Nominal line over load range, 20MHz BW; measured with 1µF and 10µF ceramic capacitor		20	120	mV_{P-P}
Rated Output Current	$I_{R-VAUX1}$				1	A
Maximum Output Capacitance	$C_{O-VAUX1}$				2	mF
Soft-Start Ramp Time	$t_{SS-VAUX1}$	All full load with max $C_{O-VAUX1}$			50	ms
VAUX3: +12V Output						
Output Voltage Set Point	$V_{SET-VAUX3}$		11.5	12	12.6	V
Output Regulation Over Line & Load					1	V
Output Voltage Ripple / Noise		Output derived directly from VS1,+12V main output; output ripple and noise depends on VS1 load; see Figures 24, 26.		40	180	mV_{P-P}
Rated Output Current	$I_{R-VAUX3}$				1	A
Maximum Output Capacitance	$C_{O-VAUX3}$				1	mF
Soft-Start Ramp Time	$t_{SS-VAUX3}$	All full load with max $C_{O-VAUX3}$			50	ms
VAUX2: +3.3V Output						
Output Voltage Set Point	$V_{SET-VAUX2}$		3.25	3.35	3.42	V
Output Regulation Over Line & Load				100	150	mV
Output Voltage Ripple / Noise		Nominal line over load range, 20MHz BW; measured with 1µF and 10µF ceramic capacitor		20	30	mV_{P-P}
Rated Output Current	$I_{R-VAUX2}$				30	A
Maximum Output Capacitance	$C_{O-VAUX2}$				9	mF
Soft-Start Ramp Time	$t_{SS-VAUX2}$	All full load with max $C_{O-VAUX2}$	5			ms

Signal Characteristics — Control Signals

The control (ENABLE*, INHIBIT*) tables are applicable over the full input/output operational range.

ENABLE*: Enable*								
• Control action for Enable* is defined in the VITA 62 control state table. • The ENABLE* pin has an internal pull-up to V_{CC} and is referenced to the SIGNAL_RETURN pin of the power supply.								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Digital Input	Any	ENABLE* Enable Threshold	$V_{ENABLE-EN}$				0.8	V
		ENABLE* Disable Threshold	$V_{ENABLE-DIS}$		2.0			V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		ENABLE* Internal Pull-Up Resistance to V_{CC}	$R_{ENABLE-INT}$		49	51	52	kΩ
		ENABLE* Enable Debounce Delay	t_{D-EN-E}		3	5		ms
		ENABLE* Disable Debounce Delay	t_{D-EN-D}		3	5		ms

INHIBIT*: Inhibit*								
• Control action for Enable* is defined in the VITA 62 control state table. • The INHIBIT* pin has an internal pull up to V_{CC} and is referenced to the SIGNAL_RETURN pin of the power supply.								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Digital Input	Any	INHIBIT* Enable Threshold	$V_{INHIBIT-EN}$	Status register bit 4 should be 0 (default) for digital input control line to have priority	2.0			V
		INHIBIT* Disable Threshold	$V_{INHIBIT-DIS}$				0.8	V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		INHIBIT* Internal Pull-Up Resistance to V_{CC}	$R_{DISABLE-INT}$		49	51	52	kΩ
		INHIBIT* Enable Debounce Delay after ENABLE*	t_{D-IN-E}		3	5		ms
		INHIBIT* Disable Debounce Delay	t_{D-IN-D}		3	5		ms
		Lockout Delay Between Consecutive INHIBIT* Enables	t_{D-IN-L}		3	5		ms

Control Signal Truth Table

VITA 62 Control States						
Signal		**Output State**				
ENABLE*	**INHIBIT***	**VS1**	**VS3**	**VAUX1**	**VAUX3**	**VAUX2**
HIGH	HIGH	OFF				
LOW	HIGH	ON				
HIGH	LOW	OFF				
LOW	LOW	OFF				ON

Signal Characteristics — Geographical Address and Monitoring

The geographical address and monitors tables are applicable over the full input/output operational range.

GA0*, GA1*, GA2*, GA3*, GA4*, GAP*: Geographical Address

- The GA0* thru GA4* pins sets the I²C™ address of the power supply. The GAP* bit provides odd parity protection over the GA[4:0]* bits. The sum of all the grounded geographical address pins, GA[4:0]* and GAP* must be odd. Global address is set at start up and cannot be changed without a power cycle.
- Each of the geographical lines has an internal pull-up to V_{CC} and is referenced to the Signal Return pin of the power supply.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Start Up	Address Pins Low Threshold	V_{ADDR-L}				0.8	V
		Address Pins High Threshold	V_{ADDR-H}		2.0			V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		ENABLE* Internal Pull-Up Resistance to V_{CC}	$R_{ADDR-INT}$		49	51	52	kΩ
		Address Pins Debounce Delay	t_{D-ADDR}		5			ms

FAIL*, SYSRESET* & LED: Monitor

- The power supply has one two-color LED located on the ejector-edge of the power supply.
- The LED is either GREEN or RED depending on the state of operation. FAIL* and SYSRESET* lines are set with the LED.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Outputs	Steady RED	SYSRESET*	V_{SYSRST}	Start up: input voltage operating threshold $V_{UV-IN} < V_{IN} < V_{OV-IN}$ has been met; if steady RED persists for >100ms, a critical system fault has been detected during start up	0.0		0.8	V
		FAIL*	V_{FAIL}		0.0		0.8	V
	Blinking GREEN	SYSRESET*	V_{SYSRST}	>100ms after $V_{UV-IN} < V_{IN} < V_{OV-IN}$ has been met; power supply is ready for use	2.0		3.5	V
		FAIL*	V_{FAIL}		2.0		3.5	V
	Steady GREEN	SYSRESET*	V_{SYSRST}	All outputs are OK and ENABLE* is pulled low	2.0		3.5	V
		FAIL*	V_{FAIL}		2.0		3.5	V
	Blinking RED	SYSRESET*	V_{SYSRST}	Power supply has encountered a OT, OV, UV, OC or critical system failure during operating	2.0		3.5	V
		FAIL*	V_{FAIL}		0.0		0.8	V
	Fast Blinking GREEN	None	-	SW priority is set by 0x55 status command	-	-	-	-
	Blinking Alternate GREEN/RED	None	-	Safety Override mode is enabled successfully by 0x55 status command	-	-	-	-

Address Assignment

I²C Address versus Geographical Address Setting

- The I²C Hardware Address (per VITA 46.11 Rev 0.15) is 7 bits.
- The default base address is 0x20.
- GA0* through GA4* provide the 5 LSB for the address.
- If the unit detects an error on the GAP* input setting, it will respond to address 0x20.

I²C Address	GA3*	GA2*	GA1*	GA0*	GAP*	GA4*
	Pin A4	Pin B4	Pin C4	Pin D4	Pin A5	Pin B5
0x20	High	High	High	High	Gnd	High
0x21				Gnd	High	
0x22			Gnd	High		
0x23				Gnd	Gnd	
0x24		Gnd	High	High	High	
0x25				Gnd	Gnd	
0x26			Gnd	High		
0x27				Gnd	High	

Application Characteristics

All of the following plots are at nominal line and 1000W aggregate load unless otherwise noted.

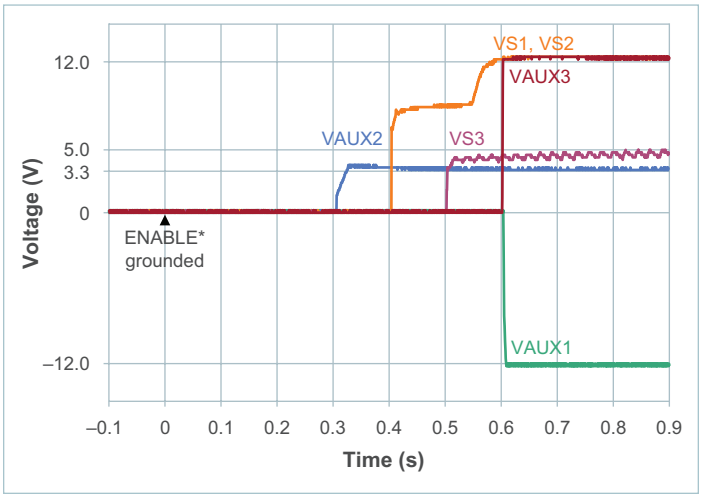


Figure 1 — *Response time from ENABLE* pin grounded to outputs available; 28V_{IN}, INHIBIT* floating, ENABLE* grounded, no load*

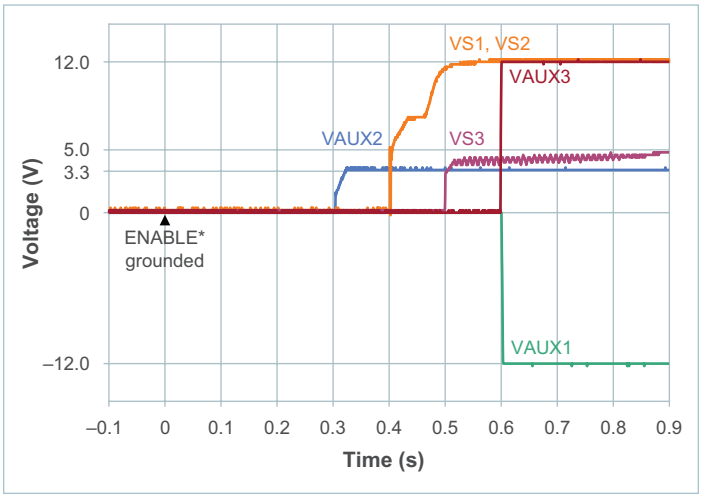


Figure 2 — *Response time from ENABLE* pin grounded to outputs available; 28V_{IN}, INHIBIT* floating, ENABLE* grounded, full load*

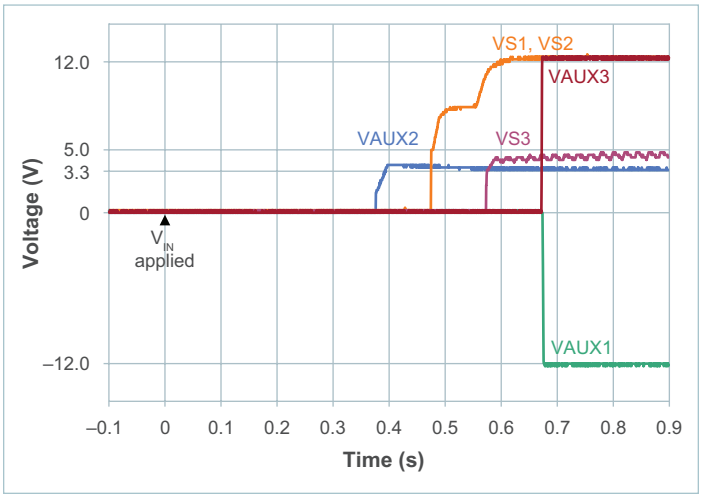


Figure 3 — *Response time from V_{IN} applied to outputs available; 28V_{IN}, INHIBIT* floating, ENABLE* grounded, no load*

Application Characteristics (Cont.)

All of the following plots are at nominal line and 1000W aggregate load unless otherwise noted.

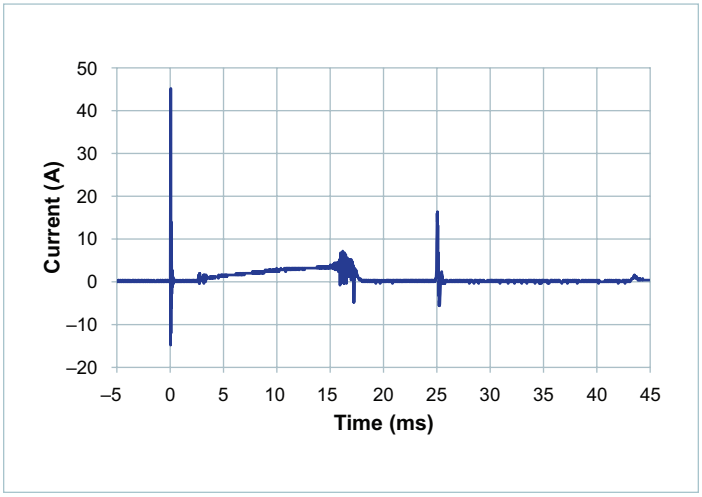


Figure 4 — *Measured inrush current at 28V input voltage, 0 – 45ms*

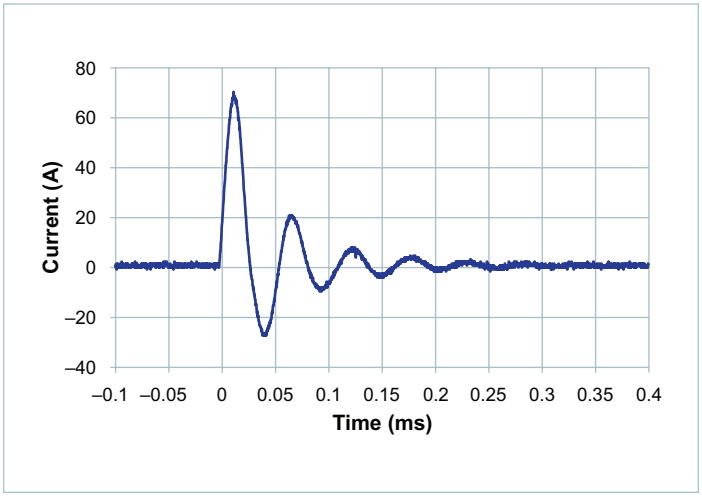


Figure 5 — *Measured inrush current at 28V input voltage, 0 – 0.4ms*

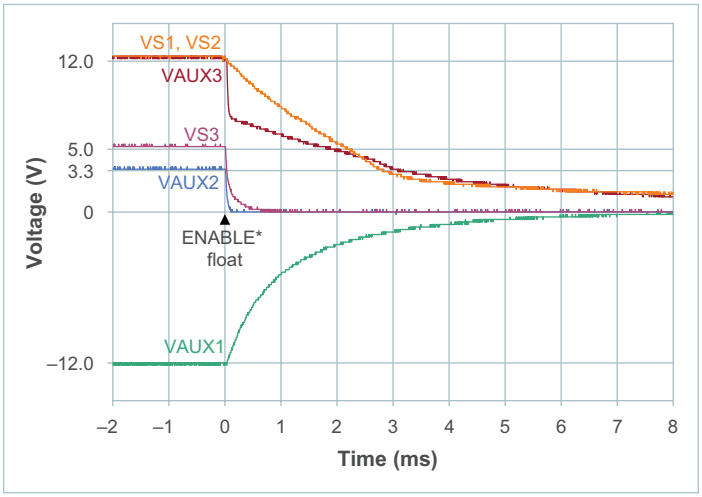


Figure 6 — *Discharge time of all outputs from ENABLE* pin moving from ground to floating, no load*

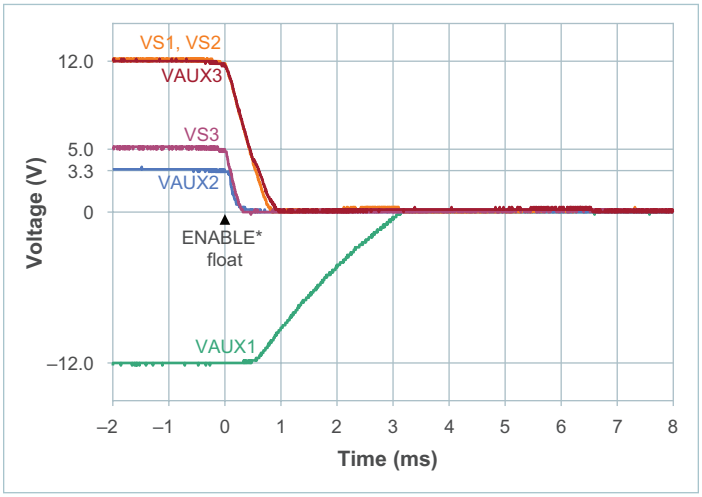


Figure 7 — *Discharge time of all outputs from ENABLE* pin moving from ground to floating, full load*

Application Characteristics (Cont.)

All of the following plots are at nominal line and 600W aggregate load unless otherwise noted.

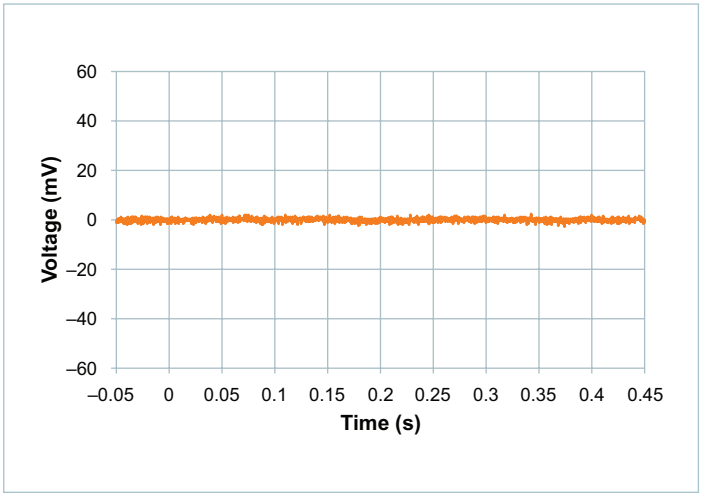


Figure 8 — *VS1 and VS2 (+12V) ripple with no load, AC-coupled*

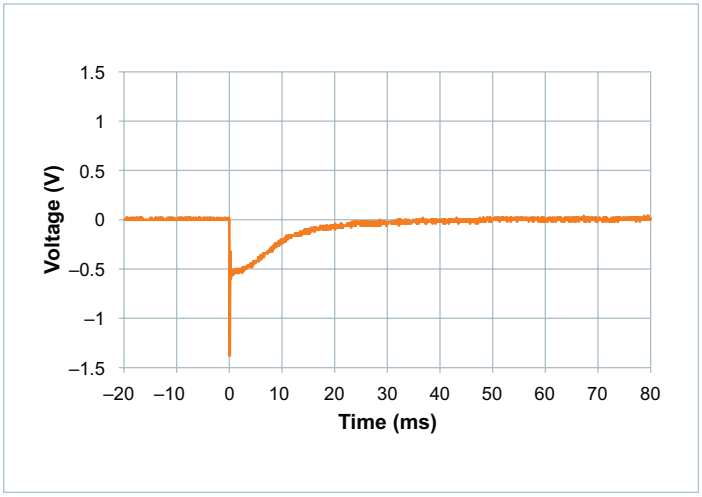


Figure 9 — *Transient response of VS1 and VS2 +12V output, load step from 0A to 70A; AC-coupled*

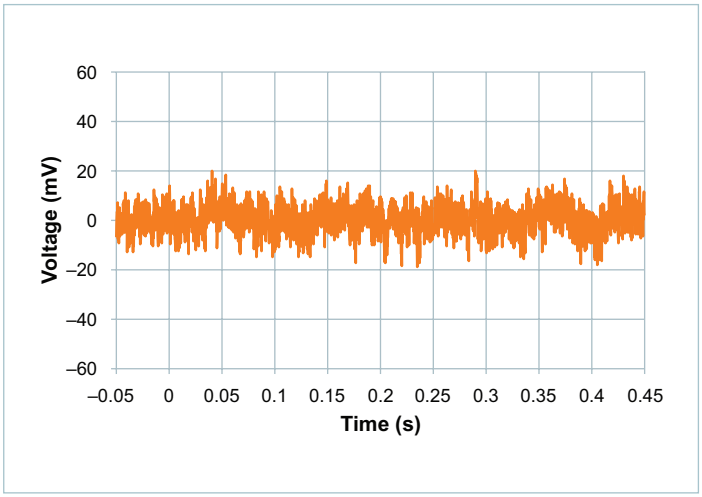


Figure 10 — *VS1 and VS2 (+12V) ripple with 70A load, AC-coupled*

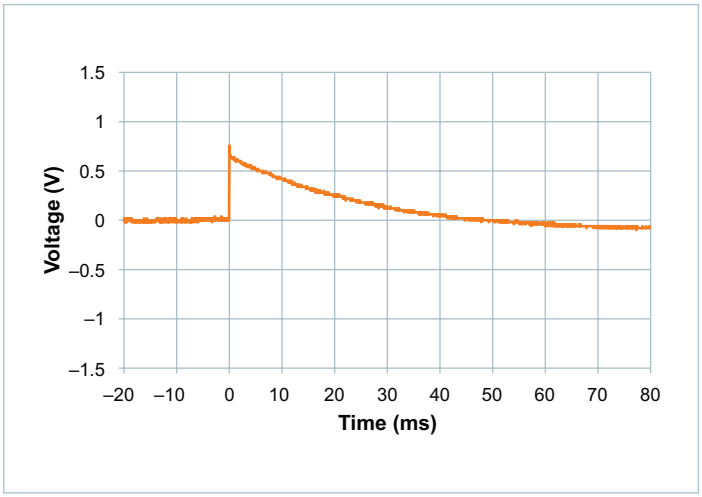


Figure 11 — *Transient response of VS1 and VS2 +12V output, load step from 70A to 0A; AC-coupled*

Application Characteristics (Cont.)

Load step response for all outputs being loaded from no load to 100% of their rated output simultaneously.

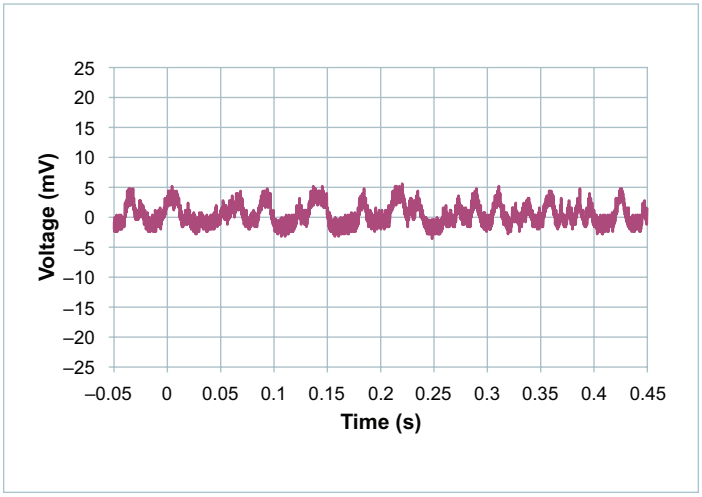


Figure 12 — *VS3 (+5V) ripple with no load, AC-coupled*

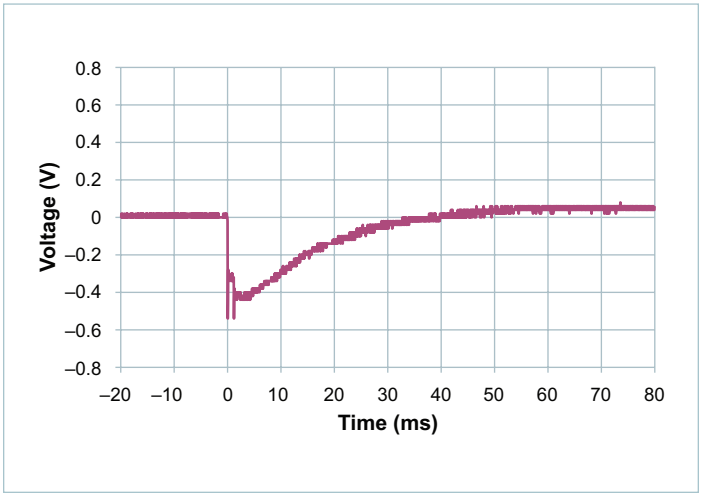


Figure 13 — *Transient response of VS3 +5V output, load step from 0A to 32A; AC-coupled*

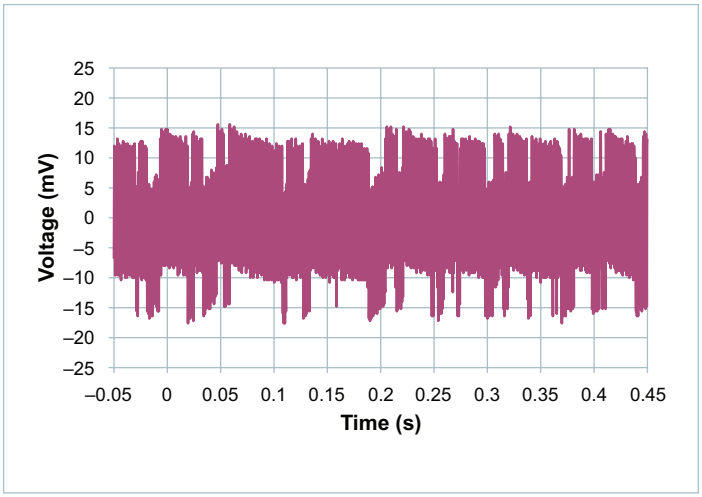


Figure 14 — *VS3 (+5V) ripple with 32A load, AC-coupled*

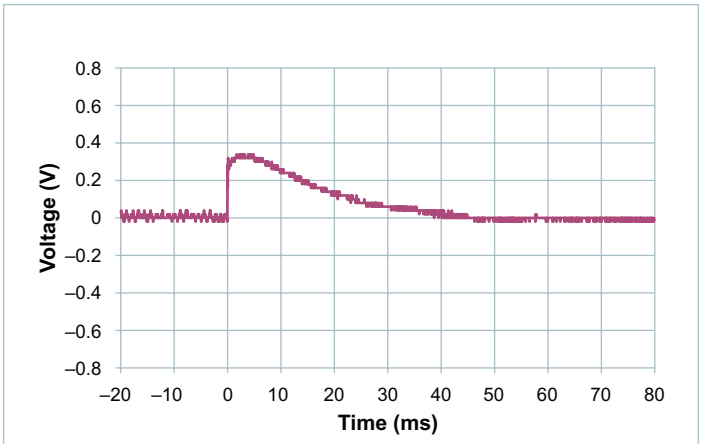


Figure 15 — *Transient response of VS3 +5V output, load step from 32A to 0A; AC-coupled*

Application Characteristics (Cont.)

Load step response for all outputs being loaded from no load to 100% of their rated output simultaneously.

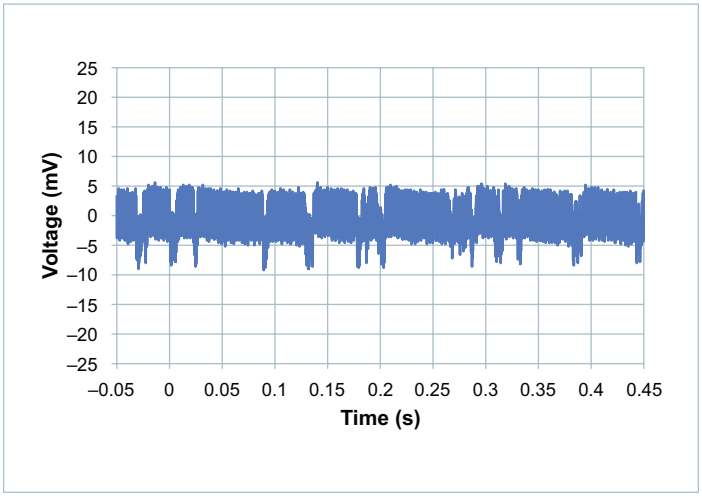


Figure 16 — *VAUX2 (+3.3V) ripple with no load, AC-coupled*

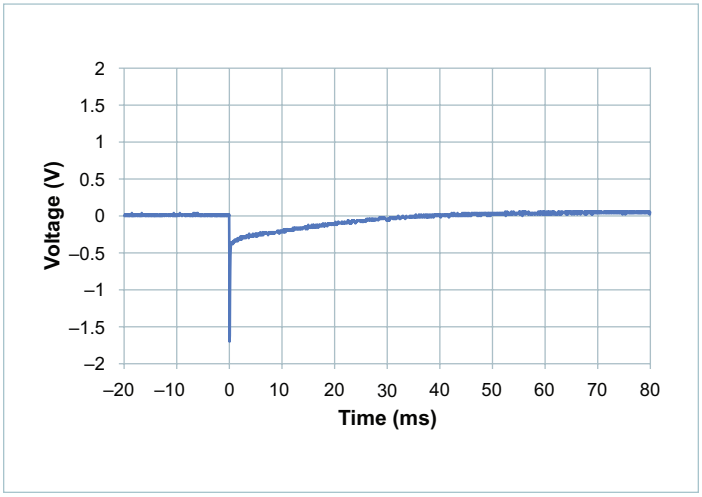


Figure 17 — *Transient response of VAUX2 +3.3V output, load step from 0A to 30A; AC-coupled*

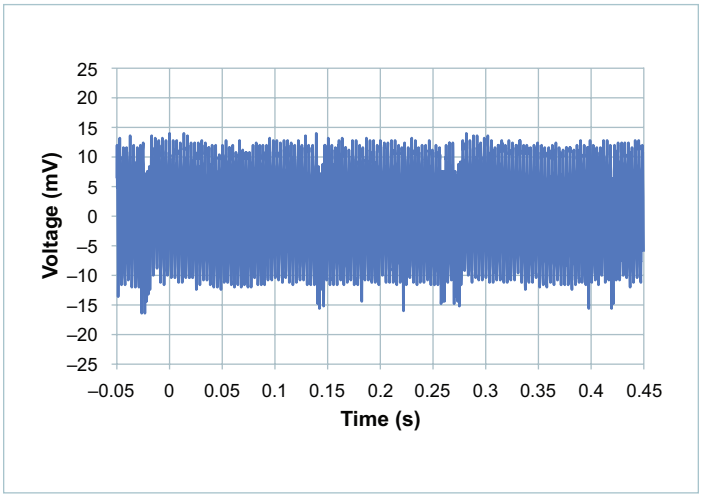


Figure 18 — *VAUX2 (+3.3V) ripple with 30A load, AC-coupled*

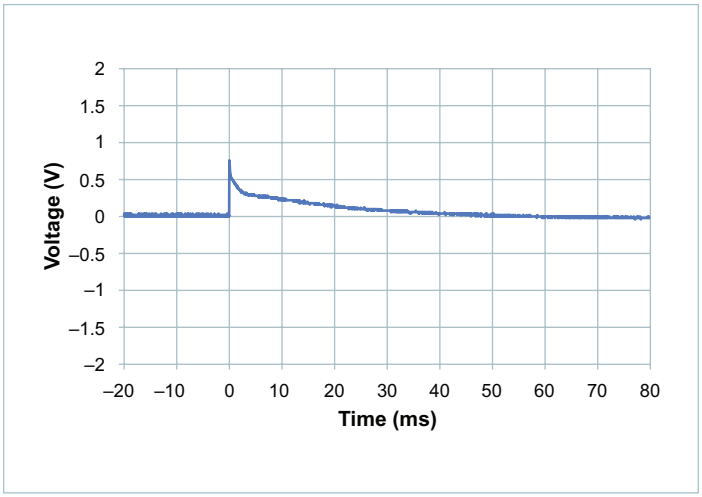


Figure 19 — *Transient response of VAUX2 +3.3V output, load step from 30A to 0A; AC-coupled*

Application Characteristics (Cont.)

Load step response for all outputs being loaded from no load to 100% of their rated output simultaneously.

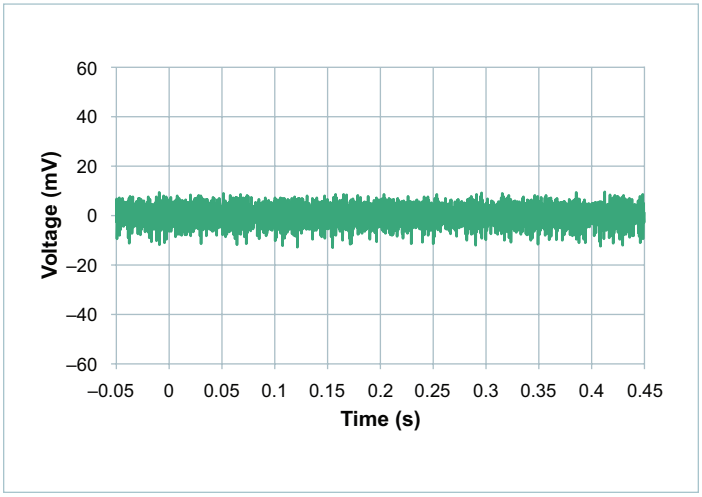


Figure 20 — *VAUX1 (–12V) ripple with no load, AC-coupled*

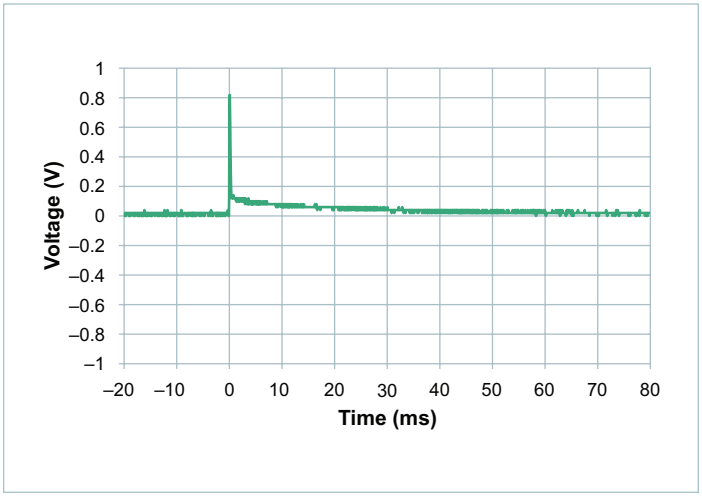


Figure 21 — *Transient response of VAUX1 –12V output, load step from 0A to 1A; AC-coupled*

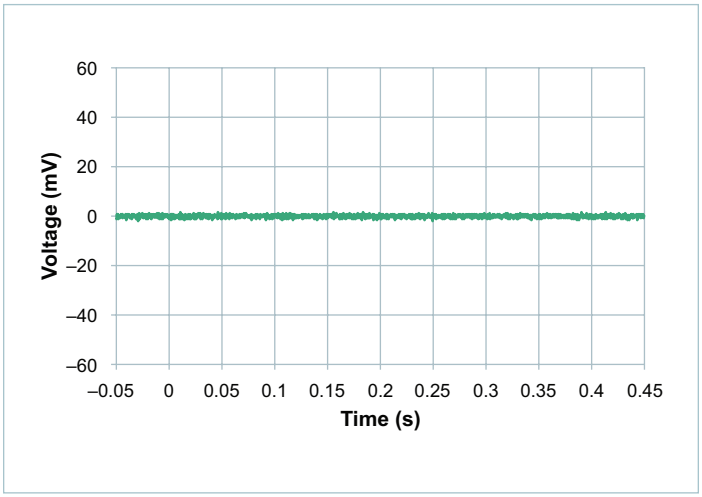


Figure 22 — *AUX1 (–12V) ripple with 1A load, AC-coupled*

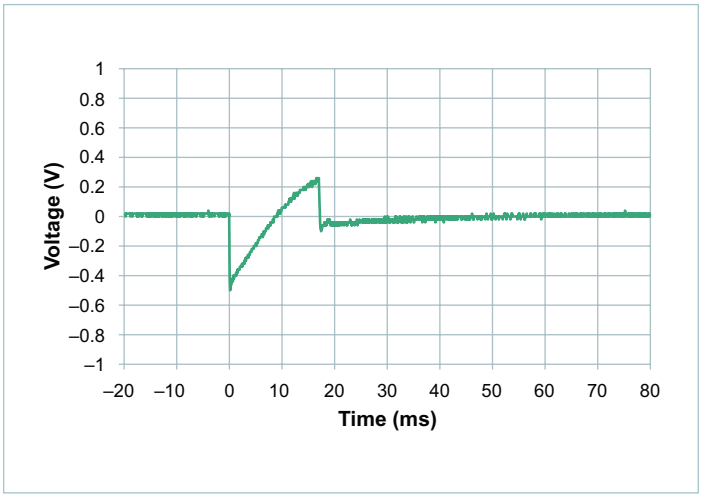


Figure 23 — *Transient response of VAUX1 –12V output, load step from 1A to 0A; AC-coupled*

Application Characteristics (Cont.)

Load step response for all outputs being loaded from no load to 100% of their rated output simultaneously.

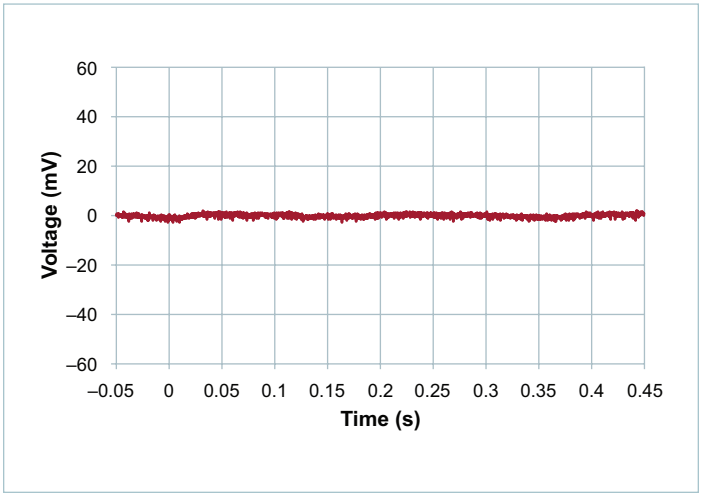


Figure 24 — *VAUX3 (+12V) ripple with no load and 5A load on VS1 and VS2 (+12V), AC-coupled*

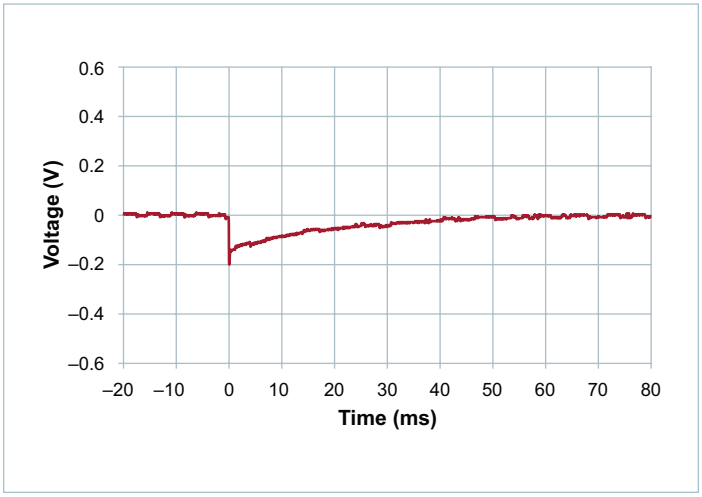


Figure 25 — *Transient response of VAUX3 +12V output, load step from 0A to 1A with 5A load on VS1 and VS2 (+12V); AC-coupled*

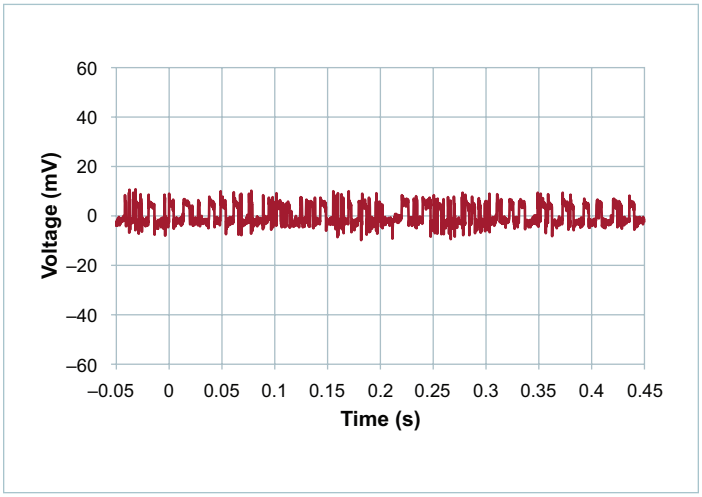


Figure 26 — *VAUX3 (+12V) ripple with 1A load, and 5A load on VS1 and VS2 (+12V), AC-coupled*

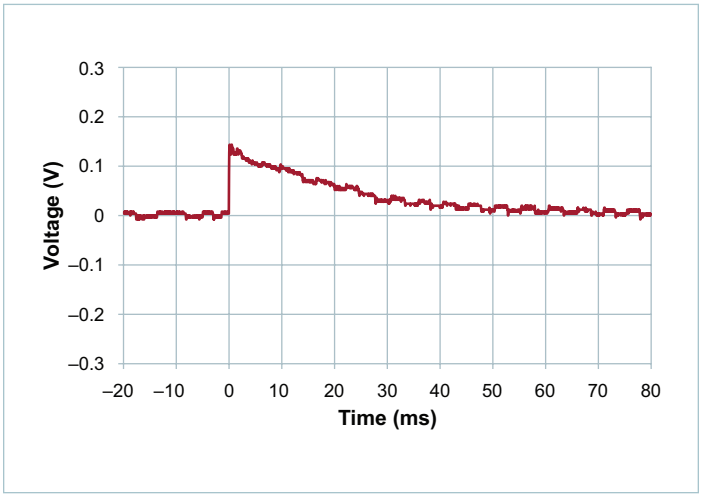


Figure 27 — *Transient response of VAUX3 +12V output, load step from 1A to 0A with 5A load on VS1 and VS2 (+12V); AC-coupled*

General Characteristics

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Per VITA62		6.634		in
Width	W	Per VITA62		9.187		in
Height	H	Per VITA62		0.951		in
Weight	W			1502		g
Wedge-Lock Torque		Manufacturer's recommended value		7		in·lbs
Thermal						
Operating Temperature	$T_{WEDGE-LOCKS}$		–40		85	°C
Assembly						
Storage Temperature			–40		125	°C
Safety						
MTBF		MIL-HDBK-217Plus Parts Count 25°C Ground Benign, Stationary, Indoors / Computer		552,647		Hrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		1,099,319		Hrs

Signal Pin Functions

ENABLE* & INHIBIT*

Enable and Inhibit pins express active low logic. See the control signal truth table on page 8 for the output state of the power supply. It is necessary to avoid the indeterminate output state where 0.8 – 2.0V is applied to the ENABLE* or INHIBIT* pins. Since the power supply has 49.9kΩ pull-up resistor to +3.3V for both lines (Enable* & Inhibit*), the floating condition for the Enable & Inhibit line will be high (logic 1).

A digital debounce filter is present on the signals of both pins to prevent false transitions. The ENABLE* and INHIBIT* also have a minimum delay between successive output enable transitions to prevent repeated starts into high-capacitance loads. See detailed specifications for delays time limits.

Geographical Address: GA0* & GA1*

Geographical address pins also exhibit active low logic. It is necessary to avoid the indeterminate state where 0.8 – 2.0V is applied to any of the address pins. Since the power supply has a 49.9K pull-up resistor to +3.3V for each of the geographical address lines, the floating condition for each of lines will be a high (logic 1).

The geographical address is static and set on power up. The power supply's address cannot change until power has been cycled and the states of the address pins have been modified before power up.

See the global address assignment table on page 9 for the geographical address assignments

I²C Ports

Both primary and redundant I²C™ ports have the same address set by the Geographical Address pins and identical functionality. There is a bidirectional buffer on both clock and data lines with internal pull ups on the IPMC and external pulls on the back plane to +3.3V are required.

FAIL*

This signal line is open drain and tracks SYSRESET* when the unit is powering up or pulled down to SIGNAL_RETURN when any of the outputs are out of specification. A pull up resistor is expected on the backplane per section 4.6.3.7 of VITA 62.

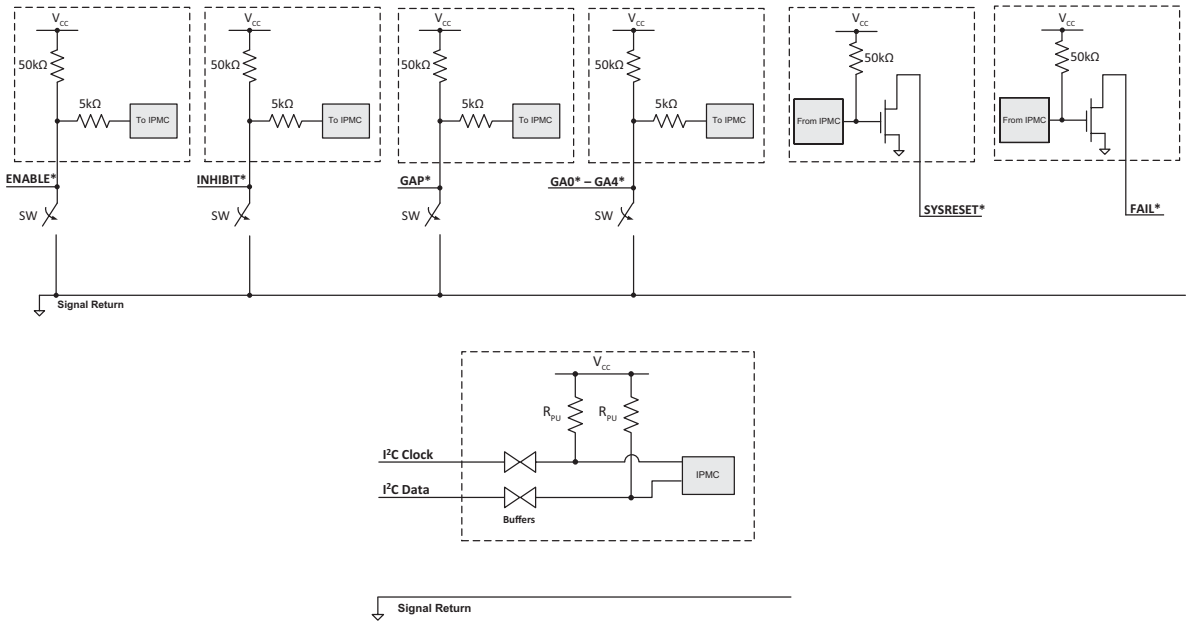
SYSRESET*

This signal line is open drain and is pulled down to SIGNAL_RETURN when the unit is powering up. The line is released when the power supply is ready for control. Appropriate pull-up/pull-down resistors are expected on the back plane per VITA 46 section 7.3.9.

SIGNAL_RETURN

SIGNAL_RETURN is used as the reference for signals pin connections and is to be tied to POWER_RETURN on the backplane per section 4.6.3.10-1 of VITA 62.

Typical External Circuits for Signal Pins (ENABLE*, INHIBIT*, GAP*, GA0* – GA4*, SYSRESET*, FAIL* and I²C Channels)



Card Edge Temperature Sensors

The PCBA card edge temperature sensor internal to the power supply is mounted on the edge of the PCBA card edge. Consequently, the temperature sensor measures a temperature that is generally higher than the heat-sink-to-rail mounting interface and lower than the hot spot of the internal converters in the power supply.

Response from the power supply to I²C™ command 0x21 provides the temperature measured by the internal sensor that reads the higher temperature. This temperature can exceed 85°C. I²C command 0x92 will respond with both PCB mounted temperature sensors.

Power Limits

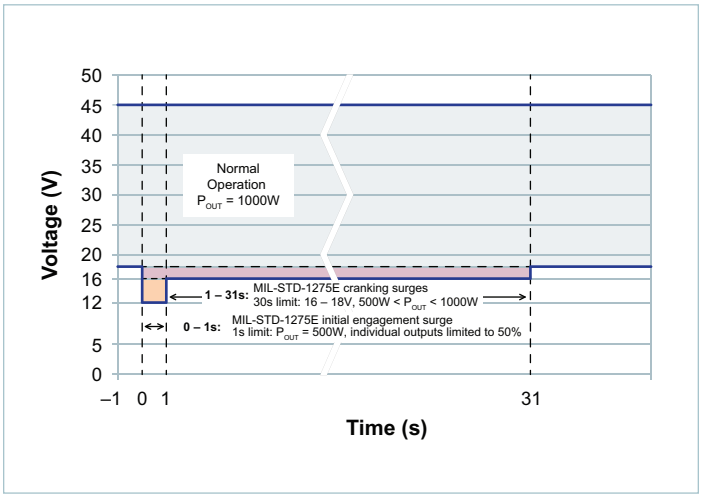


Figure 28 — *Power-time limits during transient cranking disturbances*

Per MIL-STD-1275E, the Initial Starter Engagement (ISE) can cause the nominal 28V bus to drop to 12V for a period of no more than 1s. During this time the available combined output power is required to be limited to 500W. Once the engine is cranking, the voltage will be in the range of 16 – 18V and the full combined unit power of 1000W is available but only for a maximum time of 30s due to the reduced input voltage.

If the duration at the lower voltage operation exceeds the MIL-STD-1275E maximum times, the outputs from the power supply are allowed to shut down.

Fault Operation

See Table 4 for nonrecoverable fault thresholds which trigger a fault and shut down/restart of the outputs of the supply.

Input Voltage Protection (IOVP)

If the input voltage to the power supply drops below V_{UV-IN} or exceeds V_{OV-IN} for at least 1ms, the power supply will shut down all outputs and digital communication lines until input voltage is within operating range V_{IN}. Triggering I_{OVP} has the same effect as power cycling the power supply. Supply currents and voltages are sampled every 200µs.

Output Voltage Protection (OOVP)

The power supply measures voltage from the remote-sense lines as well as the voltages on the VITA connector which do not include remote sense drop.

The FAIL* line will be asserted (pulled low) when output voltage at the connector of the power supply is greater than the nonrecoverable limit of any output. OVP will also shut down the outputs until the output voltage of the converter is within specification. The power supply will automatically restart the outputs every 1s until the fault clears.

Overcurrent Protection (OCP)*

During an overcurrent fault on any output, all outputs will shut off and the FAIL* line will be asserted. The power supply will automatically try to restart outputs every 1s if the fault has cleared.

Overtemperature Protection (OTP)

The power supply will go into overtemperature protection and shut down all outputs when either internal temperature sensor measures 95°C. The power converter will recover for normal operation when the internal temperature has dropped by 20°C.

At 85°C the Bit-5 of the Status Register (0x55) will clear if the system manager sets Bit-5 to 1 which will indicate the power supply is within 10°C from shutting down.

Parallel Operation (VS1 +12V and VS3 +5V Outputs)

For proper load regulation and paralleling of like power supplies, a single kelvin connection between each sense pin and load is required. Under normal parallel power supply operation, each supply's PoL regulated output will be at different voltage with respect to its own backplane connector to compensate for transmission voltage drop.

It is not recommended to connect the PoL sense pins in a manner in which each supply's PoL sense pins are connected to each other and also connected to each power supply's own PoL voltage output. In this case the system may appear to function normally temporarily but load regulation and sharing are not guaranteed due to the lack of a kelvin connection between the supplies and a single load point.

All five of the outputs can be connected in parallel with the same output from other identical power supplies; meaning the same part number. Only the VS1 and VS3 outputs support load sharing. If any of AUX outputs (VAUX3, VAUX1 and VAUX2) are parallel with other power supply, the maximum current rating will remain at the same rating as a single power supply.

The VS1 and VS3 outputs are configured to adjust the output voltage as a function of load.

VS1 output voltage is set to 12.120V_{DC} at no load, and the output is configured to adjust the output voltage as a function load where:

$$V_{OUT\_VS1} = 12.12V - \left(0.240V \bullet \frac{I_{OUT}}{I_{R\text{-}VS1}}\right)$$

For example: If I_{OUT} = 35A, then:

$$V_{OUT\_VS1} = 12.12V - \left(0.240V \bullet \frac{35A}{70A}\right)$$

$$= 12.00V$$

The controlled ±1% voltage droop allows the VS1 output capability to be increased by paralleling with other identical power supplies (same PN). See Table 3 for parallel-array current ratings.

Likewise, for VS3 the output voltage is set to 5.05V at no load, and the output is configured to adjust the output voltage as a function of load where:

$$V_{OUT\_VS3} = 5.05V - \left(0.100V \bullet \frac{I_{OUT}}{I_{R\text{-}VS3}}\right)$$

For example: If I_{OUT} = 16A, then:

$$V_{OUT\_VS3} = 5.05V - \left(0.100V \bullet \frac{16A}{32A}\right)$$

$$= 5.00V$$

The controlled ±1% voltage droop allows the VS3 output capability to be increased by paralleling with other identical power supplies (same PN). See Table 3 for parallel-array current ratings.

Output	Max Current vs. Paralleled Supplies				Unit
	1	2	3	4	
VS1 (+12V)	70	126	189	252	A
VS3 (+5V)	32	57.6	86.4	115.2	A
VAUX1 (–12V)	1	1	1	1	A
VAUX2 (+3.3V)	30	30	30	30	A
VAUX3 (+12V)	1	1	1	1	A

Table 3 — *Maximum current rating by output for parallel arrays*

Additional information on power supply paralleling can be found in AN:801 – Parallel Operation.

Conducted Emissions Testing

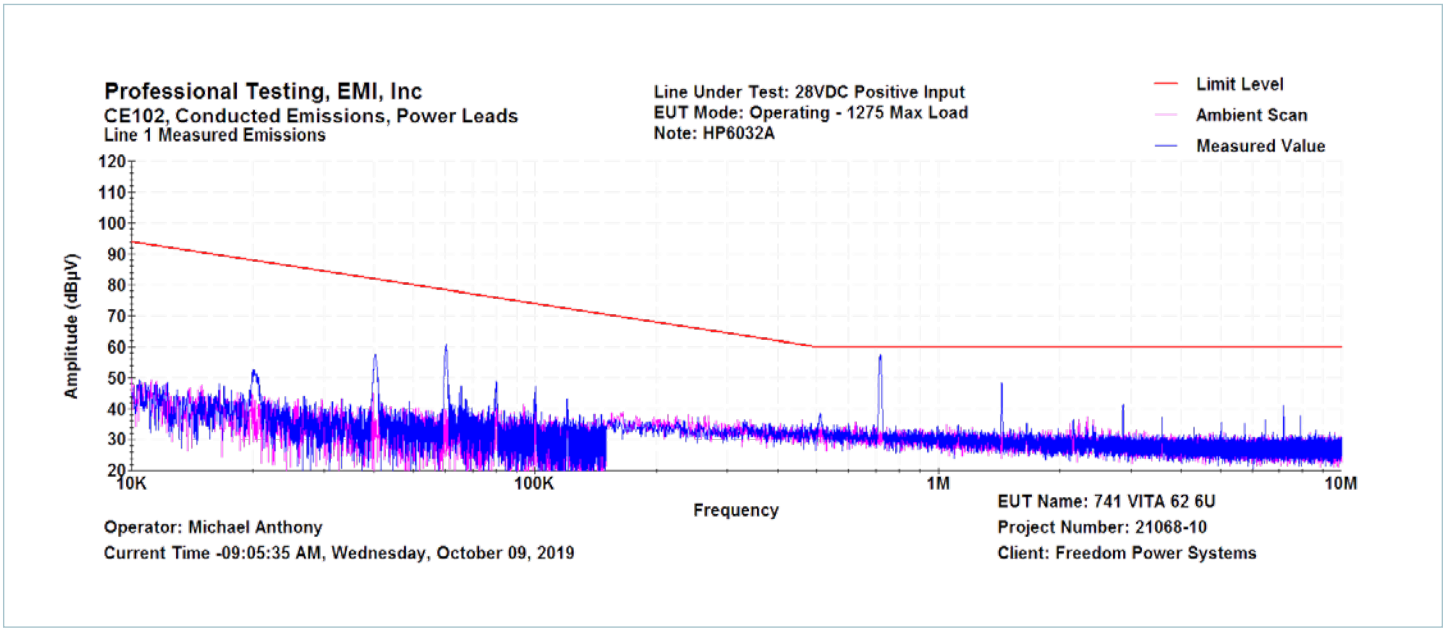


Figure 29 — *Conducted emissions of 28V_{DC} input at full load*

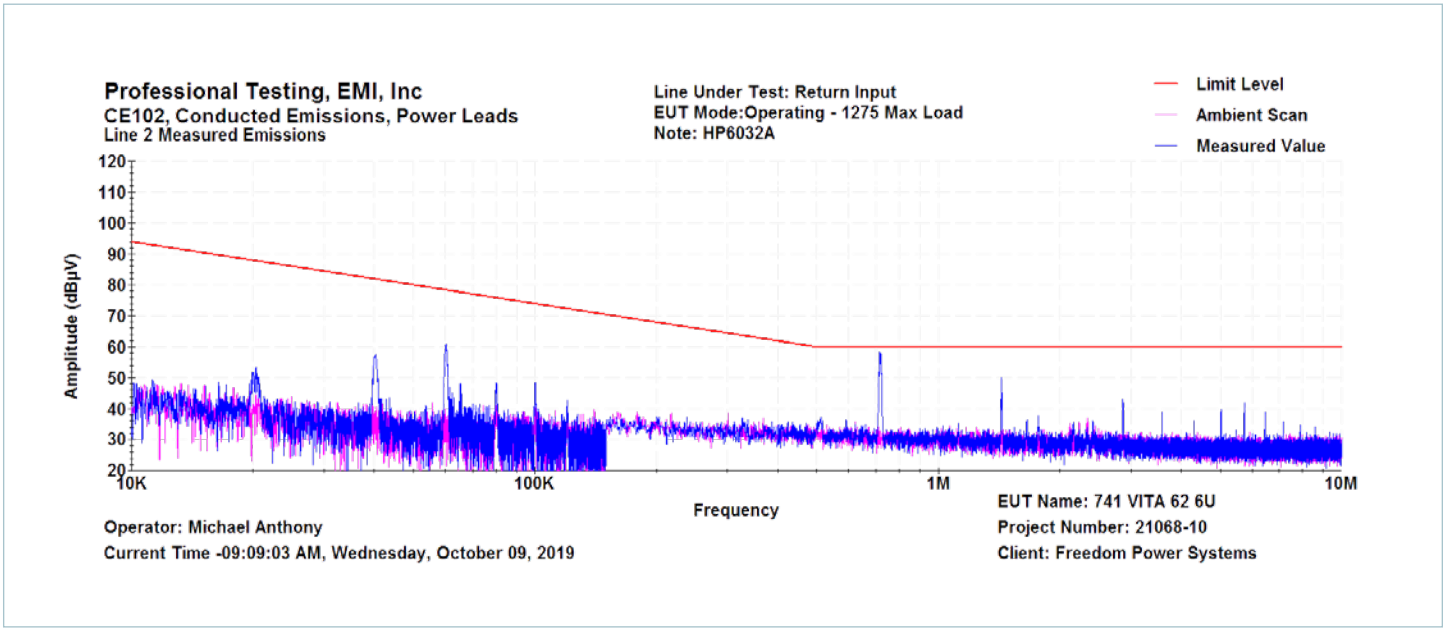


Figure 30 — *Conducted emissions of power return at full load*

Conducted Emissions Testing (Cont.)

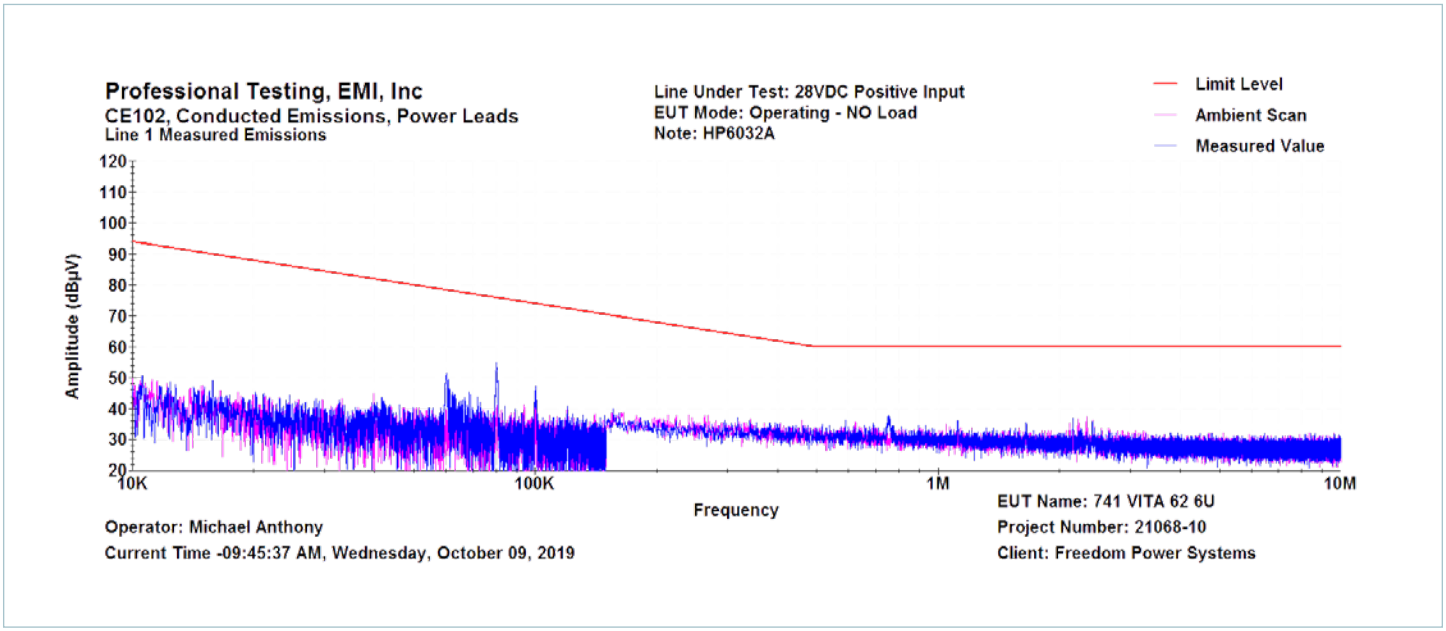


Figure 31 — *Conducted emissions of 28V_{DC} input at no load*

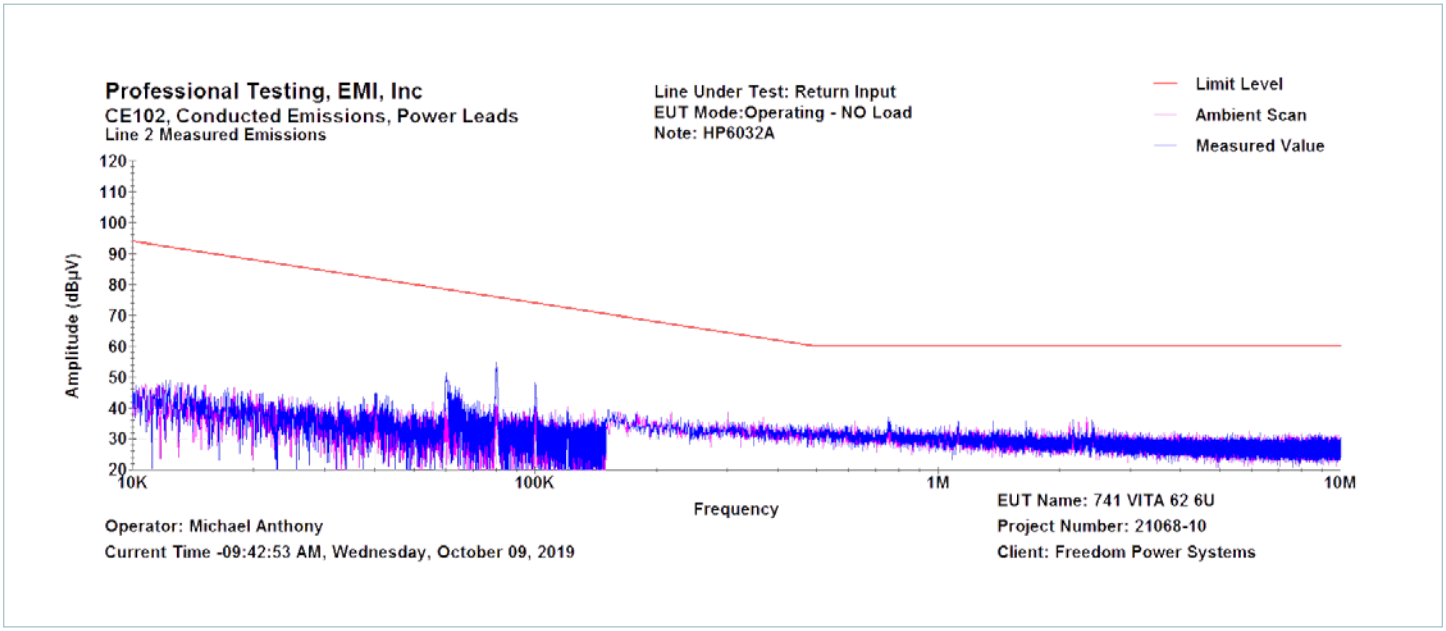


Figure 32 — *Conducted emissions of power return at no load*

Standards Compliance

MIL-STD-461G			
Section	**Test**	**Test Date**	**Results**
CE102	Conducted emissions, power leads, 10kHz to 10MHz	10/7/19	Pass
CS101	Conducted susceptibility, power leads, 30Hz to 150kHz	10/9/19	Pass
CS114	Conducted susceptibility, bulk cable injection, 10kHz to 200MHz	10/9/19	Pass
CS115	Conducted susceptibility, bulk cable injection, impulse excitation	10/28/19	Pass
CS116	Conducted susceptibility, Damped sinusoidal transients, cables and power leads, 10kHz to 100MHz	10/28/19	Pass
MIL-STD-704F per MIL-HDBK-704-8			
Section	**Test**	**Test Date**	**Results**
LDC103	Voltage distortion spectrum	10/16/19	Pass
LDC105	Normal voltage transients	10/16/19	Pass
LDC302	Abnormal voltage transients	10/16/19	Pass
MIL-STD-1275E			
Paragraph	**Test**	**Test Date**	**Results**
5.3.3.1.1	Injected voltage spikes	10/31/19	Pass
5.3.3.1.2	Emitted spikes	10/31/19	Pass
5.3.3.2.1	Injected voltage surges	10/31/19	Pass
5.3.3.2.2	Emitted voltage surges	10/31/19	Pass
5.3.4	Reverse polarity	10/31/19	Pass
5.1.1.2	Voltage ripple	11/6/19	Pass
5.1.2	Starting operation (12V at 500W operation is tested at the factory 100% of the production units). **Note:** The EUT output power rating for section 5.1.2 is 500W, and the EUT output power rating for all of other testing is 1000W.	See test column	Pass
RTCA/DO-160G			
Section	**Test**	**Test Date**	**Results**
25	Electrostatic discharge (15,000V)	11/7/19	Pass
VITA 47			
Section	**Test**	**Test Date**	**Results**
Humidity (Operational)	MIL-STD-810G, Method 507.5, Proc. II 95%RH, five 48-hour cycles	12/9-20/2019	Pass
Random Vibration (Operational)	5 – 100Hz at +3dB, 100 – 1000Hz at 0.1g^2/Hz, and 1000 – 2000Hz at 6dB, one hour per axis, 3 axes	11/13/19	Pass
Shock (Operational)	MIL-STD-810G, Method 516.6, Proc. I 40G, 11ms, 3 shocks, ± per direction, 3 axes	11/13/19	Pass
Thermal Cycling (Non-Operational)	MIL-STD-202G, Method 107G, Proc. II –40 to +105°C, 500 cycles	10/10/2019 to 11/30/2019	Pass
Altitude (Operational)	MIL-STD-810G, Method 500.5, Proc. II 60,000 feet to –15000 feet, 2 hours	11/26/19	Pass
Fungus	MIL-STD-810G, Method 508.6 28 days using fungi listed in Table 508.6-1	10/6/2019 to 11/4/2019	Pass
Corrosion Resistance	ASTM G85, Annex A4, Cycle A4.4.4.1 2 days of salt fog/SO_2 exposure	10/7/2019 to 10/9/2019	Pass

I²C™ Sensor Commands

Commands are sent by SMBus-compatible packets over the I²C physical interface. The I²C bus will communicate at 100kHz. Pull-up resistors to +3.3V are expected on the system backplane.

Six geographical address pins, labeled GAP*, GA0* – GA4* are provided at each power supply slot, where the pins are defined to be active (SET) when pulled low. See the address assignment table on page 9.

The general format is as follows:

- *Command from controller I²C / SMBus master:*

  Address+R/*W
  Command Byte
  Number of Bytes
  Zero Checksum

- *Response from power supply I²C / SMBus slave:*

  Command Echo
  Data Bytes
  Zero Checksum

Commands Recognized by Power Supply

0x21: Sensor Data (Read Only) [c]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x21	Byte	Echo of Command
1	Status Reg	Byte	Same as used by Command 0x55
2, 3	PCBA Temperature °C	UINT16	16384 = 100°C
4, 5	VS1 (+12V VSENSE)	UINT16	16384 = 12.0V
6,7	Factory Use Only	UINT16	N/A: factory use only
8, 9	+5V VSENSE	UINT16	16384 = 5.0V
10, 11	+3.3VAUX VSENSE	UINT16	16384 = 3.3V
12, 13	+12VAUX VSENSE	UINT16	16384 = 12V
14, 15	–12VAUX VSENSE	UINT16	16384 = –12V (absolute value)
16, 17	+12V IOUT	UINT16	16384 = 70
18, 19	Factory Use Only	UINT16	N/A: factory use only
20, 21	+5V IOUT	UINT16	16384 = 32
22, 23	+3.3VAUX IOUT	UINT16	16384 = 30
24, 25	+12VAUX IOUT	UINT16	16384 = 1A
26, 27	–12VAUX IOUT	UINT16	16384 = –1A (absolute value)
28, 29	Internal Reference	UINT16	N/A: factory use only
30, 31	Input Voltage	UINT16	16384 = 28.0V
32-51	Part Number	CHAR[20]	no 0 term padded with 0x20
52-55	Serial Number	UINT32	Unsigned 32-bit integer; last 9 digits of the serial number of the unit on the label
56, 57	Factory Use Only	UINT16	N/A: factory use only
58, 59	Hardware Revision	CHAR[2]	
60, 61	Firmware Revision	CHAR[2]	
62	Input Current	UINT8	255 = 128A
63	Zero Checksum	Byte	Sum(byte 0:63) = 0

[c] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Commands Recognized by Power Supply (Cont.)

0x44: Firmware Date (Read Only) [d]			
• 22 byte response in ASCII form.			
Byte Number	**Contents**	**Format**	**Typical Value**
0	0x44	Byte	Echo of the command
1 – 20	Date	ASCII[20]	'NOV 28 14:32:54 2018'
21	Zero Checksum	Byte	Sum(byte 0:20) = 0

0x45: Hardware Address (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Typical Value**
0	0x45	Byte	
1	I^2C Address	Byte	0x23
2	Zero Checksum	Byte	Sum(byte 0:2) = 0

0x55: Status Command (Read/Write) [d]			
Byte Number	**Contents**	**Format**	**Typical Value**
0	0x55	Byte	
1	Status Byte	Byte	0x18 = All outputs ON
2	Zero Checksum	Byte	Sum(byte 0:2) = 0

0x90: All Voltages in mV (Read) [d]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x21	Byte	Echo of the command
1, 2	+12V SENSE	UINT16	10mV/bit
3, 4	N/A	N/A	N/A
5, 6	+5V SENSE	UINT16	10mV/bit
7, 8	+3.3VAUX SENSE	UINT16	10mV/bit
9, 10	+12VAUX VSENSE	UINT16	10mV/bit
11, 12	–12VAUX VSENSE	UINT16	–10mV/bit
13, 14	Input Voltage	UINT16	10mV/bit
15	Zero Checksum	Byte	Sum(byte 0:14) = 0

0x99: Main Outputs – Output and Input Current in mA (Read) [d]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x99	Byte	Echo of the command
1, 2	+12V IOUT	UINT16	10mA/bit
3, 4	N/A	N/A	N/A
5, 6	+5V IOUT	UINT16	10mA/bit
7, 8	Input Current	UINT16	10mA/bit
9	Zero Checksum	Byte	Sum(byte 0:8) = 0

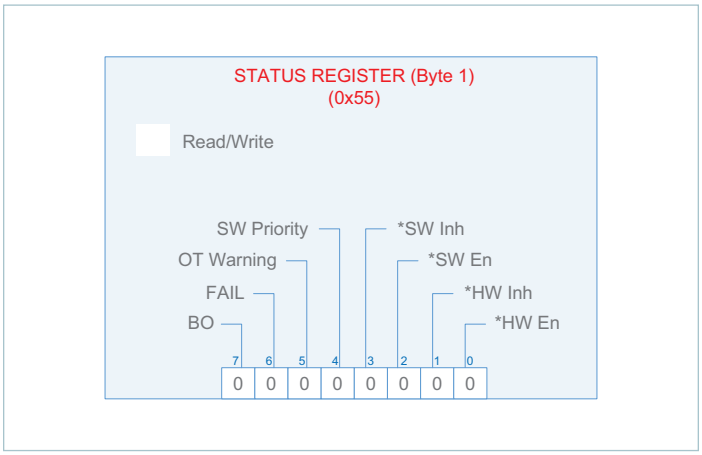
0x91: Auxiliary Outputs – Output Current in mA (Read) [d]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x91	Byte	Echo of the command
1, 2	+3.3VAUX IOUT	UINT16	1mA/bit
3, 4	+12VAUX IOUT	UINT16	1mA/bit
5, 6	–12VAUX IOUT	UINT16	–1mA/bit
7	Zero Checksum	Byte	Sum(byte 0:6) = 0

0x92: PCBA Card Edge Temperatures in °C x 10 (Read) [d]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x92	Byte	Echo of the command
1, 2	6U P0 connector, side rail	INT16	Temperature x 10, eg. –123 = –12.3°C
3, 4	6U P1 connector, side rail	INT16	Same as above
5	Zero Checksum	Byte	Sum(byte 0:4) = 0

[d] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Status Register Bit Map (Byte 1) used in command 0x55

Bit 0 and 1 allow you to monitor what the power supply is reading from the input connector.



Under some conditions, it is desirable to ignore potentially damaging conditions. For this purpose the power supply provides a safety override function in the system status register. If bit 7 in the status register is set, then any non-recoverable events that would normally shut down the supply will not do so.

Event messages are still sent, but the power supply will continue to operate until the conditions cease to exist or it fails.

In order to enable safety override mode, the command message must include the exact same data byte three times in a row within the message where normally only a single byte would be needed. See I²C guide for more details.

Bit	Name	Condition	Default
7	BO	Safety override; see description	0
6	FAIL	If set to 1 by System Manager, a fault condition will clear this bit.	0
5	OT Warning	If set to 1 by System Manager, an OT fault will clear this bit.	0
4	SW Priority	Software Priority **1** = STATUS REGISTER overrides hardware inputs for INHIBIT* and ENABLE* **0** = Hardware is in control	0
3	*SW Inh	Software Inhibit **0** = Inhibit active (same as hardware input state)	0
2	*SW En	Software Enable **0** = Enable active (same as hardware input state)	0
1	*HW Inh	As read by HW	BACKPLANE
0	*HW En	Status of INHIBIT* pin (read only)	BACKPLANE

IPMI Interface

The data interface is compliant with the requirements of VITA 46.11, VITA 62 -2016 and the IPMI v2.0 specifications. This section shows product specific information such as a sensor list and their coefficients.

Data Format

Four constants are used to calculate a real world value from the single byte variable returned in the response. The four constants are used in the equation Interpreting Received Values

$$y = \left(Mx + \left(B \bullet 10^{K1}\right)\right) \bullet 10^{K2}$$

Where:

y the converted reading

x the raw sensor reading

M the signed integer multiplier

B the signed additive offset

K1 signed exponent for constant B (sets decimal point for B)

K2 signed result exponent (sets decimal point for y)

Sensors and Constants

The list of sensors and coefficients can also be retrieved by the chassis manager by querying the "Sensor Data Record" (See VITA 46.11).

Sensor Number	Hex	Sensor Name	Type Code	Generic Event / Reading Type Code	SI Units	M	B	K1	K2	Monitor Range	Resolution
2	**0x02**	FRU Health	F2h	04h - Predictive Failure	"Digital" discrete						
3	**0x03**	FRU Voltage	02h	05h - Limit Exceeded	"Digital" discrete						
4	**0x04**	FRU Temperature	F3h	6Fh - Sensor Specific	"Digital" discrete						
7	**0x07**	Input Voltage	02h	01h - Threshold	V	20	90	1	–2	9 to 60V	0.2000
8	**0x08**	VS1, +12V Voltage	02h	01h - Threshold	V	20	90	2	–3	9 to 14.1V	0.0200
9	**0x09**	VS2, +3.3V Voltage	Not Supported								
10	**0x0A**	VS3, +5V Voltage	02h	01h - Threshold	V	10	35	2	–3	3.5 to 6.05V	0.0100
11	**0x0B**	AUX2, +3.3VAUX Voltage	02h	01h - Threshold	V	10	20	2	–3	2 to 4.55V	0.0100
12	**0x0C**	AUX3, +12VAUX Voltage	02h	01h - Threshold	V	20	90	2	–3	9 to 14.1V	0.0200
13	**0x0D**	AUX1, –12VAUX Voltage	02h	01h - Threshold	V	–20	–90	2	–3	–9 to –14.1V	0.0200
14	**0x0E**	Input Current	03h	01h - Threshold	A	4	0	0	–1	0 to 102A	0.4706
15	**0x0F**	iS1, +12V Current	03h	01h - Threshold	A	4	0	0	–1	0 to 102A	0.4706
16	**0x10**	iS2, +3.3V Current	Not Supported								
17	**0x11**	iS3, +5V Current	03h	01h - Threshold	A	20	0	0	–2	0 to 51A	0.2000
18	**0x12**	Card Edge Temp towards P1	01h	01h - Threshold	K	1	20	1	0	200 to 455K	1.0000
19	**0x13**	Card Edge Temp towards P0	01h	01h - Threshold	K	1	20	1	0	200 to 455K	1.0000
21	**0x15**	Input Power Consumption	0Bh	01h - Threshold	W	50	0	0	–1	0 to 1275W	5.0000
22	**0x16**	VS1, +12V Power Consumption	0Bh	01h - Threshold	W	40	0	0	–1	0 to 1020W	4.0000
23	**0x17**	VS2, +3.3V Power Consumption	Not Supported								
24	**0x18**	VS3, +5V Power Consumption	0Bh	01h - Threshold	W	10	0	0	–1	0 to 255W	1.0000
25	**0x19**	iAUX2, +3.3VAUX Current	03h	01h - Threshold	A	20	0	0	–2	0 to 51A	0.2000
26	**0x1A**	iAUX3, +12VAUX Current	03h	01h - Threshold	A	20	0	0	–3	0 to 5.1A	0.0200
27	**0x1B**	iAUX1, –12VAUX Current	03h	01h - Threshold	A	20	0	0	–3	0 to 5.1A	0.0200
28	**0x1C**	AUX Power Consumption	0Bh	01h - Threshold	W	10	0	0	–1	0 to 255W	1.0000

Table 3 — *Sensor list and coefficients*

Thresholds

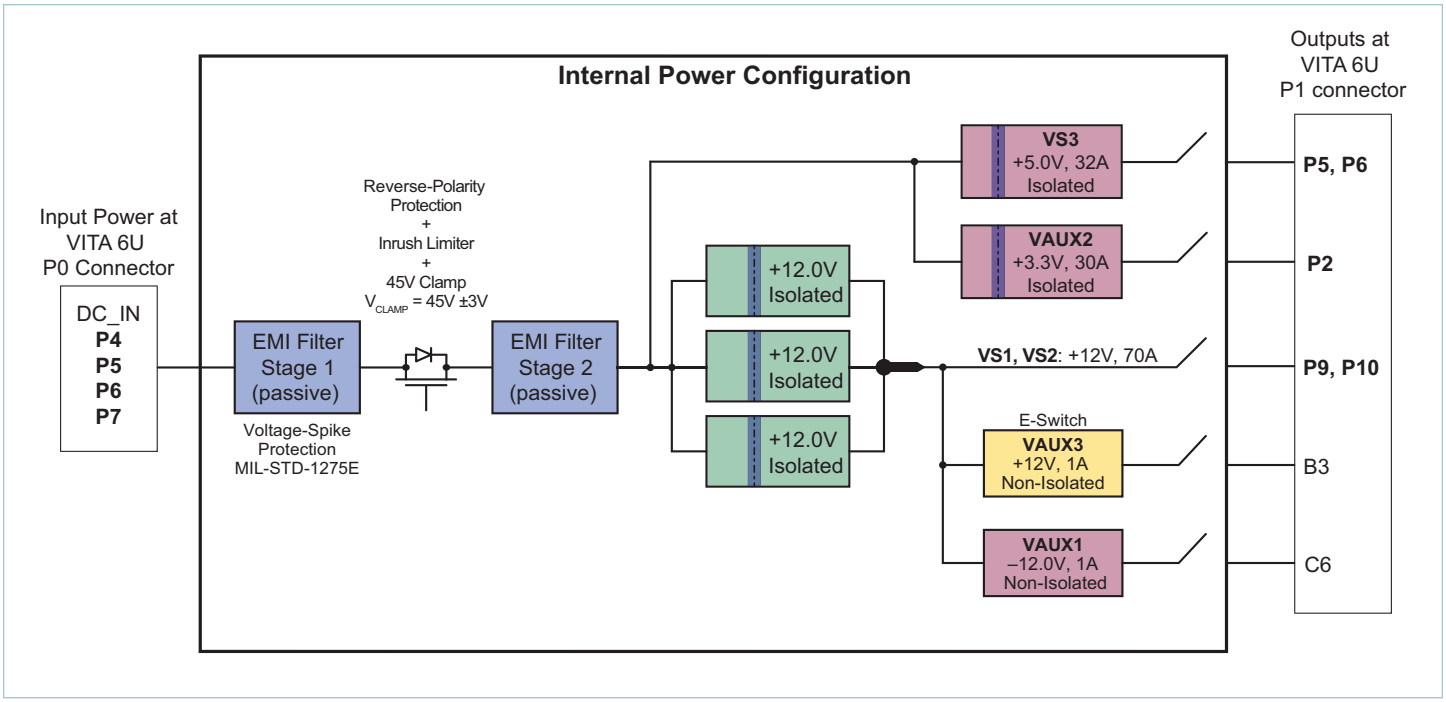
Upper and lower limits of the sensors are shown in Table 4. Exceeding the nonrecoverable or critical limits will trigger a system event message and set the appropriate bits in the warning sensor registers (Sensors 2, 3 and 4). They reflect a degradation of the power supply towards its operational limits but are still within operating norms.

Exceeding nonrecoverable limits of the power supply will cause the power supply to shut down all outputs except the 3.3V internal supply which powers the microcontroller and bus interface. The system will try to recover from all nonrecoverable faults every 1s except in the case of an overtemperature fault.

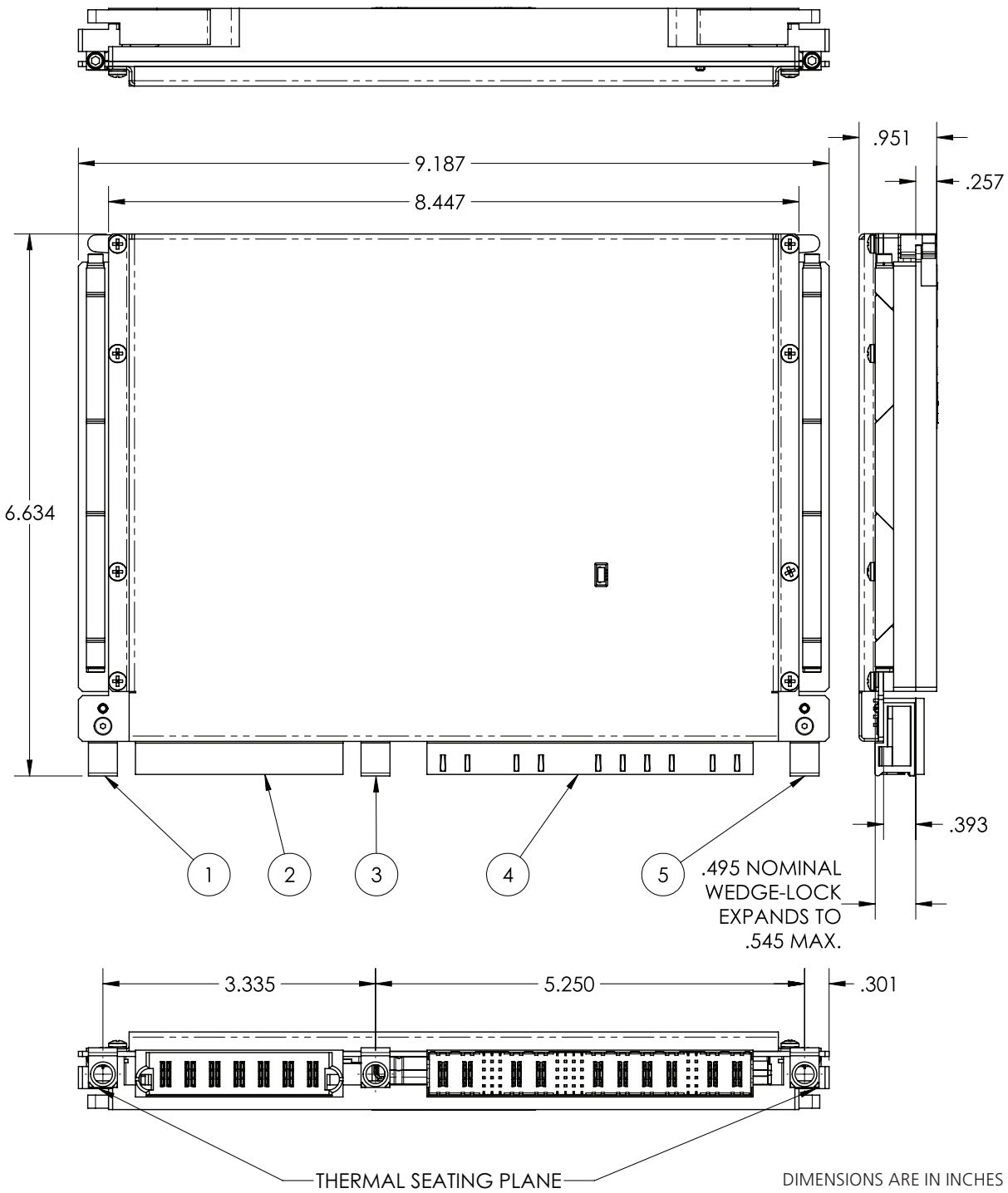
Sensors		Critical Thresholds				Nonrecoverable Thresholds				Hysteresis
		LOW		High		LOW		High		
#	Name	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count
7	Input Voltage	40	17V	155	40V	14	11.8V	166	42.2V	30
8	VS1, +12V Voltage	126	11.52V	174	12.48V	114	11.28V	187	12.74V	3
9	VS2, +3.3V Voltage	Not Supported								
10	VS3, +5V Voltage	135	4.85V	165	5.15V	130	4.8V	170	5.2V	2
11	AUX2, +3.3VAUX Voltage	124	3.24V	142	3.42V	115	3.15V	146	3.46V	1
12	AUX3, +12VAUX Voltage	124	11.48V	174	12.48V	114	11.28V	187	12.74V	4
13	AUX1, –12VAUX Voltage	126	–11.52V	174	–12.48V	114	–11.28V	187	–12.74V	4
14	Input Current			150	60A			160	64	4
15	iS1, +12V Current			175	70A			190	76	5
16	iS2, +3.3V Current	Not Supported								
17	iS3, +5V Current			160	32A			175	35	5
18	Card Edge Temp towards P6	38	238K	158	358K	32	232K	168	368K	10
19	Card Edge Temp towards P1	38	238K	158	358K	32	232K	168	368K	10
21	Input Power Consumption			227	1135W			244	1220W	4
22	VS1, +12V Power Consumption			192	768W			196	784W	4
23	VS2, +3.3V Power Consumption	Not Supported								
24	VS3, +5V Power Consumption			160	160W			170	170W	4
25	iAUX2, +3.3VAUX Current			150	30A			160	32A	3
26	iAUX3, +12VAUX Current			50	1A			65	1.3A	3
27	iAUX1, –12VAUX Current			50	1A			65	1.3A	3
28	AUX Power Consumption			123	123W			140	140W	2

Table 4 — *Sensor thresholds*

Power Architecture



Mechanical Drawing



Connector Components			
Item #	**Description**	**Manufacturer**	**Manufacturer Part Number**
1, 3, 5	VITA MULTIGIG RT GUIDE PIN 9mm	TE Connectivity	1-1469491-2
2	CONN HEADER MULTI-BEAM 7POS PCB	TE Connectivity	6450843-6
4	CONN HDR MULT-BEAM 44POS EDGE MT	TE Connectivity	6450849-6

Revision History

Revision	Date	Description	Page Number(s)
1.0	05/07/20	Initial release	n/a

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